APPENDIX:

[Note: This Appendix is provided solely for convenience; **bolded text** is used to provided guidance and/or indicate changes from Applicant's previously pending claims, and the previously-pending claim numbers 1-36 and 50-72 are used only for convenient reference.]

1. A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a chip mounting portion for mounting said semiconductor chip;

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,

a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and

a plurality of outer lead portions individually connected with said inner lead portions; and

a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;

wherein said chip mounting portion is smaller than said semiconductor chip and is positioned under a substantially central portion of said semiconductor chip, said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other and wherein said suspension leads and said chip mounting portion of said leadframe are continuously formed in an area of said semiconductor chip.

2. A semiconductor integrated circuit device according to claim 1, wherein each of said suspension leads includes a first portion and a second portion which is wider than said first portion, wherein said second portion is separated from said chip mounting portion and is positioned under said peripheral portion of said semiconductor chip, and wherein said semiconductor chip is fixed at said second portion of each of said suspension leads.

3. A semiconductor integrated circuit device according to claim 1, wherein said semiconductor chip is of a tetragonal shape.

4. A semiconductor integrated circuit device according to claim 1, wherein said semiconductor chip includes a rear surface opposing said main surface and is

fixed to said chip mounting portion and said suspension leads at one portion of said rear surface, and wherein the other portion of said rear surface which is exposed from said chip counting portion and said suspension leads is directly contacted to said resin member.

5. A semiconductor integrated circuit device according to claim 2, wherein said semiconductor chip is a rectangular shape and said suspension leads include four suspension leads, and wherein four corners of said rectangular-shaped semiconductor chip are supported by said four suspension leads.

6. A semiconductor integrated circuit device according to claim 5, wherein said resin member has a rectangular shape, and wherein said outer lead portions are extended outwardly from four sides of said rectangular-shaped resin member.

7. A semiconductor integrated circuit device according to claim 6, further comprising:

a plurality of grooves for positioning the semiconductor chip, said grooves each formed on said four suspension leads.

8. A semiconductor integrated circuit device according to claim 6, further comprising:

a plurality of projections for positioning the semiconductor chip, said projections each formed on said four suspension leads.

9. A semiconductor integrated circuit device according to claim 7, wherein said grooves are arranged on said four suspension leads so as to accord to four corners of said rectangular-shaped semiconductor chip.

10. A semiconductor integrated circuit device according to claim 8, wherein said projections are arranged on said four suspension leads so as to accord to four corners of said rectangular-shaped semiconductor chip.

11. A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a cracking suppression means for mounting said semiconductor chip thereon and for suppressing, during a reflow soldering processing, device cracking, wherein said cracking suppression means is a chip mounting portion which is smaller than said semiconductor chip and which is positioned under a substantially central portion of said semiconductor chip,

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,

a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and

a plurality of outer lead portions individually connected with said inner lead portions; and

a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;

wherein said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other and wherein said suspension leads and said chip mounting portion of said leadframe are continuously formed in an area of said semiconductor chip.

12. A semiconductor integrated circuit device according to claim 11, wherein said semiconductor chip includes a rear surface opposing said main surface and is fixed to said chip mounting portion and said suspension leads at one portion of said rear surface, and wherein the other portion of said rear surface which is exposed from said chip mounting portion and said suspension leads is directly contacted to said resin member.

13. A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a chip mounting portion for mounting said semiconductor chip,

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,

a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and

a plurality of outer lead portions individually connected with said inner lead portions; and

a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;

wherein said chip mounting portion is smaller than said semiconductor chip and is positioned under a substantially central portion of said semiconductor chip, said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and

an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other.

14. A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a cracking suppression means for mounting said semiconductor chip thereon and for suppressing, during a reflow soldering processing, device cracking, wherein said cracking suppression means is a chip mounting portion which is smaller than said semiconductor chip and which is positioned under a substantially central portion of said semiconductor chip,

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,

a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and

a plurality of outer lead portions individually connected with said inner lead portions; and

a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;

wherein said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip,

and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other.

15. A method of manufacturing a semiconductor device comprising the steps of:

(a) preparing a lead frame having a first surface and a second surface opposite to said first surface, said lead frame having a chip mounting portion, suspension leads continuously formed with said chip mounting portion and a plurality of leads each having an inner lead portion and an outer lead portion continuously formed with said inner lead portion, said first surface of said chip mounting portion being positioned to the side of said second surface of said inner lead portion of each of said plurality of leads rather than the side of said first surface of said inner lead portion of each of said plurality of leads;

(b) mounting a semiconductor chip on said chip mounting portion, said semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof and a rear surface opposite to said main surface, and having a size which is larger than that of said chip mounting portion, said semiconductor chip being mounted so that said rear surface of said semiconductor chip is faced to said first surface of said chip mounting portion;

(c) electrically connecting said inner lead portions of said plurality of leads with said bonding pads of said semiconductor chip by a plurality of bonding wires respectively, in condition that said lead frame is placed on a heat stage having a

groove for accommodating said chip mounting portion and said suspension leads and for a wire bonding operation, wherein said connecting step is performed in a condition that said chip mounting portion and said suspension leads are fitted in said groove, said rear surface of said semiconductor chip is in contact with an upper surface of said heat stage and said second surface of said chip mounting portion its spaced from a bottom surface of said groove; and

(d) sealing said semiconductor chip, said plurality of bonding wires and said chip mounting portion by a resin member.

16. A method of manufacturing a semiconductor device according to claim 15, wherein the step (a) includes bending said suspension leads, and wherein a depth of said groove is deeper than a level of said bending of said suspension leads.

17. A method of manufacturing a semiconductor device according to claim 15, wherein the step (b) includes providing an adhesive to said first surface of said chip mounting portion, wherein said semiconductor chip and said chip mounting portion are bonded to each other by said adhesive.

18. A method of manufacturing a semiconductor device according to claim 17, wherein said adhesive is not provided to said suspension leads.

19. A method of manufacturing a semiconductor device according to claim 15, wherein said plurality of leads has a first lead adjacent to one of said suspension

leads and a second lead which is relatively far from said one of said suspension leads in comparison with said first lead, and wherein a distance between the tip of said first lead and an edge of said semiconductor chip is shorter than a distance between the tip of said second lead and said edge of said semiconductor chip.

20. A method of manufacturing a semiconductor device according to claim 19, wherein a length of bonding wire connected to said first lead is shorter than a length of bonding wire connected to said second lead.

21. A method of manufacturing a semiconductor device according to claim 15, wherein a width of said chip mounting portion is larger than that of each of said suspension leads.

22. A method of manufacturing a semiconductor device according to claim 15, wherein in the step (c), parts of said inner lead portions of said plurality of leads, to which said plurality of bonding wires are bonded, are placed on said upper surface of said heat stage.

23. A method of manufacturing a semiconductor device according to claim 15, wherein said chip mounting portion has a substantially circular form in a plane view.

24. A method of manufacturing a semiconductor device according to claim 15, wherein said chip mounting portion has a substantially cross form in a plane view.

25. A method of manufacturing a semiconductor device comprising the steps of :

(a) preparing a lead frame having a first surface and a second surface opposite to said first surface, said lead frame having a chip mounting portion, suspension leads continuously formed with said chip mounting portion and a plurality of leads each having an inner lead portion and an outer lead portion continuously formed with said inner lead portion;

(b) preparing a semiconductor chip selected from among a plurality of semiconductor chips having different sizes, said semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof and a rear surface opposite to said main surface, and having a size which is larger than that of said chip mounting portion; (c) mounting said semiconductor chip on said chip mounting portion, said semiconductor chip being mounted so that said rear surface of said semiconductor chip is faced to said first surface of said chip mounting portion;

(d) electrically connecting said inner lead portions of said plurality of leads with said bonding pads of said semiconductor chip by a plurality of bonding wires, in a condition that said lead frame is placed on a heat stage having a groove for accommodating said chip mounting portion and said suspension leads and for a wire

bonding operation, wherein said connecting step is performed in condition that said chip mounting portion and said suspension leads are fitted in said groove, said rear surface of said semiconductor chip is contact with an upper surface of said heat stage and said second surface of said chip mounting portion is spaced from a bottom surface of said groove; and

(e) sealing said semiconductor chip, said plurality of bonding wires and said chip mounting portion by a resin member.

26. A method of manufacturing a semiconductor device according to claim 25, further comprising a step of bending said suspension leads such that said first surface of said chip mounting portion is located on a down side than said first surface of said inner lead portion of each of said plurality of leads in a thickness direction of said lead frame.

27. A method of manufacturing a semiconductor device according to claim 26, wherein said bending step includes providing a step portion to each of said suspension leads by said bending, and wherein a depth of said groove is deeper than a level of said bending of said suspension leads.

28. A method of manufacturing a semiconductor device according to claim 25, wherein the step (c) includes providing an adhesive to said first surface of said chip mounting portion, wherein said semiconductor chip and said chip mounting portion are bonded to each other by said adhesive.

29. A method of manufacturing a semiconductor device according to claim 28, wherein said adhesive is not provided to said suspension leads.

30. A method of manufacturing a semiconductor device according to claim 25, wherein said plurality of leads has a first lead adjacent to one of said suspension leads and a second lead which is relatively far from said one of said suspension leads in comparison with said first lead, and wherein a distance between the tip of said first lead and an edge of said semiconductor chip is shorter than a distance between the tip of said second lead and said edge of said semiconductor chip.

31. A method of manufacturing a semiconductor device according to claim 30, wherein a length of bonding wire connected to said first lead is shorter than a length of bonding wire connected to said second lead.

32. A method of manufacturing a semiconductor device according to claim 25, wherein a width of said chip mounting portion is larger than that of each of said suspension leads.

33. A method of manufacturing a semiconductor device according to claim 25, wherein in the step (e), parts of said inner lead portions of said plurality of leads, to which said plurality of bonding wires are bonded, are placed on said upper surface of said heat stage.

34. A method of manufacturing a semiconductor device according to claim 25, wherein said chip mounting portion has a substantially circular form in a plane view.

35. A method of manufacturing a semiconductor device according to claim 25, wherein said chip mounting portion has a substantially cross form in a plane view.

36. A method of manufacturing a semiconductor device comprising the steps of;

(a) preparing a lead frame having a first surface and a second surface opposite to said first surface, said lead frame having a chip mounting portion, suspension leads continuously formed with said chip mounting portion and a plurality of leads each having an inner lead portion and an outer lead portion continuously formed with said inner lead portion, said first surface of said chip mounting portion being positioned to the side of said second surface of said inner lead portion of each of said plurality of leads rather than the side of said first surface of said inner lead portion of each of said plurality of leads;

(b) mounting a semiconductor chip on said chip mounting portion, said semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof and a rear surface opposite to said main surface, and having a size which is larger than that of said chip mounting portion, said

semiconductor chip being mounted so that said rear surface of said semiconductor chip is faced to said first surface of said chip mounting portion;

(c) electrically connecting said inner lead portions of said plurality of leads with said bonding pads of said semiconductor chip by a plurality of bonding wires respectively, in condition that said lead frame is placed on a heat stage having a groove for accommodating said chip mounting portion and said suspension leads and for a wire bonding operation, wherein said connecting step is performed in a condition that said chip mounting portion and said suspension leads are fitted in said groove, said rear surface of said semiconductor chip is in contact with an upper surface of said heat stage and said second surface of said chip mounting portion and said suspension leads arc spaced from a bottom surface of said groove; and

(d) sealing said semiconductor chip, said plurality of bonding wires and said chip mounting portion by a resin member.

37-49. (Canceled)

50. A semiconductor device comprising:

(a) a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof;

(b) a lead frame having:

a chip mounting portion for mounting said semiconductor chip;

a plurality of leads each having an inner lead portion and an outer lead portion continuously formed with said inner lead portion and arranged at a periphery of said chip mounting portion;

suspension leads continuously formed with said chip mounting portion, said semiconductor chip being mounted on said chip mounting portion;

(c) an insulating tape adhered to said inner lead portions of said plurality of leads and said suspension leads;

(d) bonding wires electrically connected to said inner lead portions of said plurality of leads with said bonding pads of said semiconductor chip respectively, and

(e) a resin member sealing said semiconductor chip, said bonding wires, said insulating tape, said chip mounting portion, a part of each of said suspension leads, and said inner lead portions of said plurality of leads,

wherein a size of said chip mounting portion is smaller than that of said semiconductor chip, and

wherein said insulating tape continuously extends from said inner lead portions of said plurality of leads to said suspension leads.

51. A semiconductor device according to claim 50, wherein said resin member has a rectangular shape, wherein said suspension leads extend from said chip mounting portion toward four corners of said resin member, and wherein said inner lead portions of said plurality of leads are arranged between said suspension leads in a plane view.

52. A semiconductor device according to claim 50, wherein said insulating tape extends along four sides of said resin member to surround said chip mounting portion and said semiconductor chip in a plane view.

53. A semiconductor device according to claim 50, wherein said insulating tape includes a base insulating film and an adhesive layer applied to one surface of said base insulating film, and wherein said insulating tape is adhered to said inner lead portions and said suspension leads by said adhesive layer.

54. A semiconductor device according to claim 53, wherein said base insulating film includes a polyimide resin and said adhesive layer includes an acrylic resin.

55. A semiconductor device according to claim 50, wherein said lead frame having a first surface and a second surface opposite to said first surface, wherein each of said suspension leads has a step portion so that said first surface of said chip mounting portion is positioned to the side of said second surface of said inner lead portion of each of said plurality of leads rather than the side of said first surface of said inner lead portion of each of said plurality of leads, and wherein said insulating tape is arranged outside said step portion of each of said suspension leads.

56. A semiconductor device according to claim 55, wherein a part of each of said suspension leads, which is located outside said step portion, is substantially at a same level as said inner lead portions of said plurality of leads in a thickness direction of said lead frame.

57. A semiconductor device comprising:

(a) a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof and a rear surface opposite to said main surface;

(b) a lead frame having a first surface and a second surface opposite to said first surface, said lead frame having:

a chip mounting portion for mounting said semiconductor chip;

suspension leads continuously formed with said chip mounting portion;

a plurality of leads each having an inner lead portion and an outer lead portion continuously formed with said inner lead portion and being arranged at a periphery of said chip mounting portion;

(c) a plurality of bonding wires electrically connected to said inner lead portions of said plurality of leads with said bonding pads of said semiconductor chip respectively; and

(d) a resin member sealing said semiconductor chip, said bonding wires, said chip mounting portion and said inner lead portions of said plurality of leads,

wherein a size of said chip mounting portion is smaller than that of said semiconductor chip,

wherein said semiconductor chip is mounted on said chip mounting portion, such that said rear surface of said semiconductor chip is bonded to the side of said first surface of said chip mounting portion by an adhesive layer, and such that a part of each of said suspension leads, which is located under said semiconductor chip, is spaced from said rear surface of said semiconductor chip.

58. A semiconductor device according to claim 57, wherein said adhesive layer is provided on said first surface of said chip mounting portion and is not provided on said part of each of said suspension leads which is located under said semiconductor chip.

59. A semiconductor device according to claim 58, wherein a part of said rear surface of said semiconductor chip, which is located outside said chip mounting portion, is adhered to a part of said resin member.

60. A semiconductor device according to claim 59, wherein said resin member includes a thermosetting resin.

61. A semiconductor device according to claim 57, wherein said adhesive layer includes an epoxy resin.

62. A semiconductor device comprising:

(a) a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof and a rear surface opposite to said main surface;

(b) a lead frame having a first surface and a second surface opposite to said first surface, said lead frame having:

a chip mounting portion for mounting said semiconductor chip;

suspension leads continuously formed with said chip mounting portion;

a plurality of leads each having an inner lead portion and an outer lead portion continuously formed with said inner lead portion and being arranged at the periphery of said chip mounting portion;

(c) a plurality of bonding wires electrically connected to said inner lead portions of said plurality of leads with said bonding pads of said semiconductor chip respectively; and

(d) a resin member sealing said semiconductor chip, said bonding wires, said chip mounting portion and said inner lead portions of said plurality of leads,

wherein a size of said chip mounting portion is smaller than that of said semiconductor chip,

wherein said semiconductor chip is bonded to said chip mounting portion by an adhesive layer between said rear surface of said semiconductor chip and said first surface of said chip mounting portion,

wherein each of said suspension leads has a part which is located under said semiconductor chip, and

wherein a part of said resin member is formed between said part of each of said suspension leads and said rear surface of said semiconductor chip.

63. **(Amendments from prior version indicated in bold)** A semiconductor device comprising:

(1) a semiconductor chip having a main surface and a rear surface opposite to said main surface, said semiconductor chip having a plurality of semiconductor elements and bonding pads formed on said main surface;

(2) a lead frame including:

a first suspension lead for supporting said semiconductor chip, extending in a first direction;

a second suspension lead for supporting said semiconductor chip, extending in a second direction which is different from said first direction, said second suspension lead intersecting said first suspension lead; and

a plurality of leads each having an inner lead and an outer lead which is continuously formed with said inner lead, said plurality of leads being arranged to surround an intersecting portion of said first and second suspension leads;

(3) a plurality of bonding wires electrically connecting said inner leads of said plurality of leads with said plurality of bonding pads, respectively; and

(4) a resin body sealing said semiconductor chip, said inner leads of said plurality of leads, said first and second suspension leads and said plurality of bonding wires;

wherein said semiconductor chip is disposed on **and supported by a flag-less** said intersecting portion of said first and second suspension leads, **with said first and second suspension leads being unitarily formed with one another,**

wherein a width of each of said first and second suspension leads **supporting said semiconductor chip** at the vicinity of said intersecting portion is wider than that of each said first and second suspension leads at vicinities beyond said semiconductor chip, **and widened portions of said first and second suspension leads are smaller than said semiconductor chip,** and

wherein said rear surface of said semiconductor chip is fixed to said first and second suspension leads **by an adhesive at at least two shift-preventing positions separated from each other. ~~at the vicinity of said intersecting point by an adhesive.~~**

64. A semiconductor device according to claim 63, wherein said first and second suspension leads intersect each other at a substantially right angle.

65. A semiconductor device according to claim 64, wherein said resin body has a tetragonal shape, wherein said outer leads of said plurality of leads protrude outwardly from four sides of said resin body, and wherein said first and second suspension leads extend from said intersecting portion toward four corners of said resin body.

66. A semiconductor device according to claim 63, wherein a portion of said rear surface of said semiconductor chip is adhered to said intersecting portion of said first and second suspension leads, and wherein another portion of said rear surface of said semiconductor chip is contacted with said resin body.

67. A semiconductor device according to claim 64, wherein said semiconductor chip has a tetragonal shape, and wherein said wider portion at the vicinity of said intersecting portion of said first and second suspension leads extends from a central portion of said rear surface of said semiconductor chip toward four corners of said semiconductor chip.

68. **(Amendments from prior version indicated in bold)** A semiconductor device comprising:

(1) a semiconductor chip having a main surface and a rear surface opposite to said main surface, said semiconductor chip having a plurality of semiconductor elements and bonding pads formed on said main surface;

(2) a lead frame including:

a chip mounting portion for mounting said semiconductor chip, **wherein said chip mounting portion is smaller than said semiconductor chip**;

a plurality of suspension leads which are ~~continuously~~ **unitarily** formed with said chip mounting portion; and

a plurality of leads each having an inner lead and an outer lead which is continuously formed with said inner lead, said plurality of leads being arranged to surround said chip mounting portion;

(3) a plurality of bonding wires electrically connecting said inner leads of said plurality of leads with said plurality of bonding pads, respectively; and

(4) a resin body sealing said semiconductor chip, said inner leads of said plurality of leads, said chip mounting portion, said plurality of suspension leads and said plurality of bonding wires;

wherein said chip mounting portion has a first portion extending in a first direction and a second portion extending in a second direction which is a different direction from said first direction, said second portion intersecting said first portion,

wherein a width of each of said first and second portions of said chip mounting portion is wider than that of each of said plurality of suspension leads,

wherein both ends of each of said first and second portions of said chip mounting portion are coupled with said plurality of suspension leads respectively,

wherein an intersecting portion of said first and second portions of said chip mounting portion is located at a substantially central portion of said rear surface of said semiconductor chip,

wherein said both ends of each of said first and second portions of said chip mounting portion are located ~~at~~ **toward** the peripheral portions of said rear surface of said semiconductor chip, and

wherein said rear surface of said semiconductor chip is fixed to said chip mounting portion **by an adhesive at at least two shift-preventing positions**

separated from each other. ~~**at both of said central and peripheral portions of said rear surface of said semiconductor chip by an adhesive.**~~

69. A semiconductor device according to claim 68, wherein said first and second directions intersect each other at a substantially right angle.

70. A semiconductor device according to claim 69, wherein said resin body has a tetragonal shape, wherein said outer leads of said plurality of leads protrude outwardly from four sides of said resin body, and wherein said plurality of suspension leads extend from said both ends of said first and second portions of said chip mounting portion toward four corners of said resin body.

71. A semiconductor device according to claim 68, wherein a portion of said rear surface of said semiconductor chip is adhered to said first and second portions of said chip mounting portion, and wherein another portion of said rear surface of said semiconductor chip is contacted with said resin body.

72. A semiconductor device according to claim 71, wherein said semiconductor chip has a tetragonal shape, and wherein said both ends of each of said first and second portions are located at the vicinity of four corners of said semiconductor chip.

73. **(Substantially parallels claim 1; differences indicated in bold)** A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a chip mounting portion for mounting said semiconductor chip;

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,

a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and

a plurality of outer lead portions individually connected with said inner lead portions; and

a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;

wherein said chip mounting portion is smaller than said semiconductor chip and is positioned under a substantially central portion of said semiconductor chip, said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of ~~each~~ **at least one** of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of ~~each~~ **said at least one** of said suspension leads and said

semiconductor chip are **positionally** separated from each other, and wherein said suspension leads and said chip mounting portion of said leadframe are continuously formed in an area of said semiconductor chip.

74. **(Substantially parallels claim 11; differences indicated in bold)** A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a cracking suppression means for mounting said semiconductor chip thereon and for suppressing, during a reflow soldering processing, device cracking, wherein said cracking suppression means is a chip mounting portion which is smaller than said semiconductor chip and which is positioned under a substantially central portion of said semiconductor chip,

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,

a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and

a plurality of outer lead portions individually connected with said inner lead portions; and

a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;

wherein said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of ~~each~~ **at least one** of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of ~~each~~ **said at least one** of said suspension leads and said semiconductor chip are **positionally** separated from each other, and wherein said suspension leads and said chip mounting portion of said leadframe are continuously formed in an area of said semiconductor chip.

75. **(Substantially parallels claim 13; differences indicated in bold)** A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a chip mounting portion for mounting said semiconductor chip,

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,

a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and

a plurality of outer lead portions individually connected with said inner lead portions; and

a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;

wherein said chip mounting portion is smaller than said semiconductor chip and is positioned under a substantially central portion of said semiconductor chip, said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of ~~each~~ **at least one** of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and

an adhesive region of ~~each~~ **said at least one** of said suspension leads and said semiconductor chip are **positionally** separated from each other.

76. **(Substantially parallels claim 14; differences indicated in bold)** A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a cracking suppression means for mounting said semiconductor chip thereon and for suppressing, during a reflow soldering processing, device cracking, wherein said cracking suppression means is a chip mounting portion

which is smaller than said semiconductor chip and which is positioned under a substantially central portion of said semiconductor chip,

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,

a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and

a plurality of outer lead portions individually connected with said inner lead portions; and

a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;

wherein said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of **~~each~~ at least one** of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of **~~each~~ said at least one** of said suspension leads and said semiconductor chip are **positionally** separated from each other.